AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Previously presented) A semiconductor memory comprising:

a first conductivity type semiconductor substrate;

one or more memory cells comprising an island-like semiconductor layer, a charge storage layer and a control gate, the charge storage layer and the control gate being formed to entirely or partially encircle a sidewall of the island-like semiconductor layer,

wherein an active region of at least one of said memory cells is electrically insulated from the semiconductor substrate by:

a second conductivity type impurity diffusion layer formed in the semiconductor substrate or in the island-like semiconductor layer, and

means for forming a depletion layer formed at a junction between the second conductivity type impurity diffusion layer and the semiconductor substrate or the island-like semiconductor layer.

2. (Canceled)

3. (Previously presented) A semiconductor memory according to claim 1, wherein a plurality of memory cells are formed with regard to one island-like semiconductor layer.

4. (Canceled)

5. (Previously presented) A semiconductor memory comprising:

a first conductivity type semiconductor substrate;

one or more memory cells comprising an island-like semiconductor layer, a charge storage layer and a control gate, the charge storage layer and the control gate being formed to entirely or partially encircle a sidewall of the island-like semiconductor layer,

wherein an active region of at least one of said memory cells is electrically insulated from the semiconductor substrate; and

wherein a plurality of memory cells are formed with regard to one island-like semiconductor layer, and the active region of at least one of the memory cells is electrically insulated from another memory cell by:

a second conductivity type impurity diffusion layer formed in the semiconductor substrate or the island-like semiconductor layer, and

means for forming a depletion layer formed at a junction between the second conductivity type impurity diffusion layer and the semiconductor substrate or the island-like semiconductor layer.

6. (Canceled)

7. (Original) A semiconductor memory according to claim 1, wherein a plurality of memory cells are formed with regard to one island-like semiconductor layer and the memory cells are arranged in series.

8. (Original) A semiconductor memory according to claim 1, wherein

a plurality of island-like semiconductor layers are formed in matrix,

impurity diffusion layers for reading a state of a charge stored in a memory cell are formed in the island-like semiconductor layers,

a plurality of control gates are provided continuously in a direction to form a control gate line and

a plurality of the impurity diffusion layers in a direction crossing the control gate line are connected to form a bit line.

9. (Original) A semiconductor memory according to claim 1, wherein a gate electrode for selecting a memory cell is formed at least at an end of the memory cell formed on the island-like semiconductor layer so as to partially or entirely encircle the sidewall of the island-like semiconductor layer and the gate electrode is arranged in series with the memory cell.

10. (Canceled)

11. (Previously presented) A semiconductor memory according to claim 1, wherein a plurality of memory cells are formed with regard to one island-like semiconductor layer and control gates constituting the memory cell are arranged so closely that channel layers of memory cells are electrically connected.

12. (Previously presented) A semiconductor memory according to claim 9, wherein the control gate and the gate electrode are disposed so closely that a channel layer located in a part of

the island-like semiconductor layer opposed to the gate electrode is electrically connected to a channel layer of the memory cell.

13. (Previously presented) A semiconductor memory according to claim 1, wherein a plurality of memory cells are formed with regard to one island-like semiconductor layer, and an electrode for electrically connecting channel layers of memory cells is further formed between control gates.

14. (Previously presented) A semiconductor memory according to claim 9, wherein a plurality of memory cells are formed with regard to one island-like semiconductor layer, and an electrode for electrically connecting a channel layer located in a part of the island-like semiconductor layer opposed to the gate electrode to a channel layer of the memory cell is further formed between the control gate and the gate electrode.

15. (Previously presented) A semiconductor memory according to claim 9, wherein all, some or one control gate(s) are formed of the same material as all, some or one gate electrode(s).

16. (Previously presented) A semiconductor memory according to claim 9, wherein the charge storage layer and the gate electrode are formed of the same material.

17. (Original) A semiconductor memory according to claim 1, wherein a plurality of island-like semiconductor layers are formed in matrix, and the width of the island-like

semiconductor layers in one direction is smaller than a distance between adjacent island-like semiconductor layers in the same direction.

18. (Original) A semiconductor memory according to claim 1, wherein a plurality of island-like semiconductor layers are formed in matrix, and a distance between the island-like semiconductor layers in one direction is smaller than a distance between the island-like semiconductor layers in another direction.

19. (Previously presented) A semiconductor memory comprising:

a first conductivity type semiconductor substrate;

one or more memory cells comprising an island-like semiconductor layer, a charge storage layer and a control gate, the charge storage layer and the control gate being formed to entirely or partially encircle a sidewall of the island-like semiconductor layer,

wherein an active region of at least one of said memory cells is electrically insulated from the semiconductor substrate; and

wherein a lower gate electrode of a first selection transistor, the control gate of the memory cell, and an upper gate electrode of a second selection transistor are arranged in an upward order in a direction vertical to the semiconductor substrate, so that the first and second selection transistors are located on opposite vertical sides of the memory cell in a vertical direction so as to sandwich the memory cell therebetween.

20-28. (Canceled)

29. (Previously presented) The semiconductor memory of claim 1, wherein the control gate and the charge store layer each laterally surround a portion of the sidewall of the island-like semiconductor layer on all lateral sides thereof.

30. (Canceled)

31. (Previously presented) The semiconductor memory of claim 1, wherein the impurity diffusion layer is formed in a top portion of the semiconductor substrate immediately under the island-like semiconductor layer.

32. (Previously presented) The semiconductor memory of claim 1, wherein the island-like semiconductor layer is pillar-shaped so as to have a height dimension greater than a width dimension.

33. (Previously presented) The semiconductor memory of claim 32, wherein the island-like semiconductor layer has a circular cross section when viewed from above.

34. (Previously presented) The semiconductor memory of claim 1, wherein the semiconductor memory is an EEPROM.

35. (Previously presented) The semiconductor memory of claim 1, wherein said sidewall of the island-like semiconductor layer is vertically extending relative to a surface of the semiconductor substrate.

36. (Previously presented) A semiconductor memory comprising:

a first conductivity type semiconductor substrate;

at least one memory cell comprising an island-like semiconductor layer, a charge storage layer and a control gate, wherein the charge storage layer and the control gate entirely or partially laterally surround at least a portion of a sidewall of the island-like semiconductor layer;

wherein the active region of said memory cell is electrically insulated from the semiconductor substrate by:

a second conductivity type impurity diffusion layer formed in the semiconductor substrate or in the island-like semiconductor layer, and

means for forming a depletion layer formed at a junction between the second conductivity type impurity diffusion layer and the semiconductor substrate or the island-like semiconductor layer.

37. (Previously presented) A semiconductor memory according to claim 19, wherein said active region of said memory cell is electrically insulated from the semiconductor substrate by at least a second conductivity type impurity diffusion layer formed in the semiconductor substrate or in the island-like semiconductor layer.

38. (Previously presented) A semiconductor memory according to claim 19, wherein the active region of said memory cell is electrically insulated from the semiconductor substrate by:

a second conductivity type impurity diffusion layer formed in the semiconductor substrate or in the island-like semiconductor layer, and

a depletion layer formed at a junction between the second conductivity type impurity diffusion layer and the semiconductor substrate or the island-like semiconductor layer.

39. (Previously presented) The semiconductor memory of claim 36, wherein the control gate and the charge store layer each laterally surround at least said portion of the sidewall of the island-like semiconductor layer on all lateral sides thereof.

40. (Previously presented) The semiconductor memory of claim 36, wherein the diffusion layer is formed at a bottom portion of the island-like semiconductor layer.

41. (Previously presented) The semiconductor memory of claim 36, wherein the island-like semiconductor layer is pillar-shaped so as to have a height dimension greater than a width dimension.

42. (Previously presented) The semiconductor memory of claim 41, wherein the island-like semiconductor layer has a circular cross section when viewed from above.

43. (Previously presented) The semiconductor memory of claim 36, wherein the semiconductor memory is an EEPROM.

44. (Previously presented) The semiconductor memory of claim 36, wherein said sidewall of the island-like semiconductor layer is vertically extending relative to a surface of the semiconductor substrate.

45. (Previously presented) The semiconductor memory of claim 36, wherein a plurality of memory cells are stacked on top of one another over the semiconductor substrate and each use the island-like semiconductor layer, and wherein respective active regions of each of the memory cells are electrically insulated from the semiconductor substrate.

46. (Previously presented) A semiconductor memory comprising:

a first conductivity type semiconductor substrate;

at least one memory cell comprising a pillar-shaped semiconductor layer having a height dimension greater than a width dimension, a charge storage layer and a control gate, wherein the charge storage layer and the control gate entirely or partially laterally surround at least a portion of a sidewall of the pillar-shaped semiconductor layer, wherein the sidewall of the pillar-shaped semiconductor layer extends vertically relative to the semiconductor substrate;

wherein at least a portion of the pillar-shaped semiconductor layer of the memory cell is electrically insulated from the semiconductor substrate by:

a second conductivity type impurity diffusion layer formed in the semiconductor substrate or in the pillar-shaped semiconductor layer, and

means for forming a depletion layer formed at a junction between the second conductivity type impurity diffusion layer and the semiconductor substrate or the pillar-shaped semiconductor layer.

47-48 (Canceled)

49. (Previously presented) The semiconductor memory of claim 46, wherein the control gate and the charge store layer each laterally surround at least said portion of the sidewall of the pillar-shaped semiconductor layer on all lateral sides thereof.

50. (Previously presented) The semiconductor memory of claim 46, wherein the pillar-shaped semiconductor layer has a circular cross section when viewed from above.

51. (Previously presented) The semiconductor memory of claim 46, wherein the semiconductor memory is an EEPROM.

52. (Previously presented) The semiconductor memory of claim 46, wherein a plurality of memory cells are stacked on top of one another over the semiconductor substrate and each use the pillar-shaped semiconductor layer, and wherein respective active regions of each of the memory cells are electrically insulated from the semiconductor substrate.

53. (Previously presented) The semiconductor memory of claim 1, wherein the semiconductor substrate is an SOI board.

54. (Previously presented) The semiconductor memory of claim 1, wherein a lower gate electrode of a first selection transistor, the control gate of the memory cell, and an upper gate electrode of a second selection transistor are arranged in an upward order in a direction vertical to the semiconductor substrate, so that the first and second selection transistors are located on opposite vertical sides of the memory cell in a vertical direction.

55. (Previously presented) A semiconductor memory comprising:

a first conductivity type semiconductor substrate;

a plurality of stacked memory cells, on top of each other, each memory cell comprising an island-like semiconductor layer, a charge storage layer and a control gate, the charge storage layer and the control gate being formed to entirely or partially encircle a sidewall of the island-like semiconductor layer,

wherein an active region of at least one of said memory cells is electrically insulated from the semiconductor substrate; and

wherein a lower gate electrode of a first selection transistor, the control gates of the plurality of memory cells, and an upper gate electrode of a second selection transistor are arranged in an upward order in a direction vertical to the semiconductor substrate, so that the first and second selection transistors are located on opposite vertical sides of the plurality of memory cells in a vertical direction so as to sandwich the plurality of memory cells therebetween.

56. (Previously presented) A semiconductor memory according to claim 55, wherein said active region of at least one of said memory cells is electrically insulated from the semiconductor substrate by:

at least a second conductivity type impurity diffusion layer formed in the semiconductor substrate or in the island-like semiconductor layer, and

a depletion layer formed at a junction between the second conductivity type impurity diffusion layer and the semiconductor substrate or the pillar-shaped semiconductor layer.

57. (New) The memory of claim 46, wherein a lower gate electrode of a first selection transistor, control gates of a plurality of memory cells, and an upper gate electrode of a second selection transistor are arranged in an upward order in a direction vertical to the semiconductor substrate, so that the first and second selection transistors are located on opposite vertical sides of the plurality of memory cells in a vertical direction so as to sandwich the plurality of memory cells therebetween.